Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) The method of claim ~~1~~ 5, wherein the ~~first~~ signal is a direct stream digital (DSD) signal.

3. (Currently Amended) The method of claim ~~1~~ 5, wherein the ~~second signal is a~~ multiple bit values are pulse code modulated (PCM) ~~signal~~ values.

4. (Cancelled)

5. (Currently Amended) A method for conversion of signals, comprising:

receiving a first plurality of bits from a signal;

performing a look-up in a table with a first subset of bits in the first plurality of bits to generate a result;

adding the result to generate a sum;

performing another look-up in the table with a second subset of bits in the first plurality of bits and adding the result to the sum until a look-up with a last subset of bits in the first plurality of bits is performed and the result added to the sum, ~~The method of claim 4,~~ wherein the table is a two dimensional array containing a plurality of elements, the size of the first dimension equal ~~the~~ a number of bits in the plurality of bits divided by ~~the~~ a number of bits in the subset of the plurality of bits, the size of the second dimension equal to $2^{(\text{number of bits in subset})}$,

outputting the sum as a first multiple bit value; and

receiving a second plurality of bits from the signal and converting to a second multiple bit value using the steps described above until all bits in the signal have been converted, wherein each plurality of bits has the same number of bits and each subset of bits in the plurality of bits has the same number of bits.

6. (Currently Amended) The method of claim 5, wherein each element contains one multiple bit result, wherein performing the look-up in the table comprises accessing the element in the array that corresponds to the number of the subset in the plurality of bits and ~~the~~ a value of the subset of bits.

7. (Currently Amended) A method for conversion of direct stream digital (DSD) signals to pulse code modulated (PCM) signals, comprising:

receiving a first plurality of bits from the DSD signal;

performing a look-up in a table with a first word in the first plurality of bits to generate a result;

adding the result to generate a sum;

performing another look-up in the table with a second word in the first plurality of bits and adding the result to the sum until a look-up with a last word in the first plurality of bits is performed and the result added to the sum;

~~providing~~ outputting the sum as a first multiple bit PCM value ~~of a PCM signal~~; and

receiving a second plurality of bits from the DSD signal and converting to a second multiple bit PCM value ~~of the PCM signal~~ using the steps described above until all bits in the DSD signal have been converted.

8. (Previously Presented) The method of claim 7, wherein each plurality of bits has the same number of bits and each word in the plurality of bits has the same number of bits.

9. (Currently Amended) The method of claim 8, wherein the table is a two dimensional array containing a plurality of elements, the size of the first dimension equal ~~the~~ a number of bits in the plurality of bits divided by ~~the~~ a number of bits in the word, the size of the second dimension equal to $2^{(\text{number of bits in word})}$.

10. (Currently Amended) The method of claim 9, wherein each element contains one multiple bit result, wherein performing the look-up in the table comprises accessing the element in the array that corresponds to the number of the word in the plurality of bits and ~~the~~ a value of the word.

11. (Cancelled)

12. (Currently Amended) An apparatus for conversion of signals, comprising:

a first-in-first-out (FIFO) buffer that contains a plurality of bits from a signal, wherein the plurality of bits is further divided into a plurality of subset of bits of the same size;

a look-up table coupled to the FIFO buffer, wherein the look-up table generates a result for each of the plurality of subset of bits;

an accumulator coupled to the look-up table, the accumulator holding the results added together, wherein after adding the result for the last subset of bits in the plurality of bits, the accumulator generates at an output a multiple bit value; and ~~The apparatus of Claim 11, further comprising~~ an address generator connected to the FIFO buffer and look-up table, said address generator providing to the look-up table ~~the~~ an address of a section in the look-up table corresponding to each of the plurality of subset of bits, each of said sections including a plurality of results for each subset of bits, wherein ~~the~~ a value of the subset of bits selects one of the plurality of results.

13. (Currently Amended) The apparatus of ~~Claim~~ claim 12, wherein the address of each section in the look-up table corresponding to each of the plurality of subset of bits is sequential.

14. (Currently Amended) The apparatus of ~~Claim 11~~ claim 12, wherein the ~~first~~ signal is a direct stream digital (DSD) signal.

15. (Currently Amended) The apparatus of ~~Claim 11~~ claim 12, wherein the ~~second signal~~ multiple bit value is a pulse code modulated (PCM) ~~signal~~ value.

16. (Currently Amended) The apparatus of ~~Claim 11~~ claim 12, wherein the look-up table is contained in a memory located on a digital signal processor (DSP).

17. (Currently Amended) The apparatus of ~~Claim 11~~ claim 12, wherein the look-up table is contained in an external memory coupled to a digital signal processor (DSP).

18. (Original) An apparatus for conversion of direct stream digital (DSD) signals to pulse code modulated (PCM) signals, comprising:

a first-in-first-out (FIFO) buffer that contains a plurality of bits from the DSD signal, wherein the plurality of bits is further divided into a plurality of words of the same size;

a look-up table coupled to the FIFO buffer, wherein the look-up table generates a result for each word; and

an accumulator coupled to the look-up table, the accumulator holding the results added together, wherein after adding the result for the last word in the plurality of bits, the accumulator generates at an output a multiple bit PCM signal.

19. (Currently Amended) The apparatus of ~~Claim~~ claim 18, further comprising an address generator connected to the FIFO buffer and look-up table, said address generator providing to the look-up table ~~the~~ an address of a section in the look-up table corresponding to each of the plurality of words, each of said sections including a plurality of results for each word, wherein ~~the~~ a value of the word selects one of the plurality of results.

20. (Currently Amended) The apparatus of ~~Claim~~ claim 18, wherein the look-up table is contained in a memory located on a digital signal processor (DSP).

21. (Currently Amended) The apparatus of ~~Claim~~ claim 18, wherein the look-up table is contained in an external memory coupled to a digital signal processor (DSP).

22. (Currently Amended) An apparatus for conversion of signals, comprising:

means for receiving a first plurality of bits from a ~~first~~ signal;

means for performing a look-up in a table with a first subset of bits in the first plurality of bits to generate a result;

means for adding the result to generate a sum;

means for performing another look-up in the table with a second subset of bits in the first plurality of bits and adding the result to the sum until a look-up with a last subset of bits in the first plurality of bits is performed and the result added to the sum, wherein the table is a two dimensional array containing a plurality of elements, the size of the first dimension equal a number of bits in the plurality of bits divided by a number of bits in the subset of the plurality of bits, the size of the second dimension equal to $2^{(\text{number of bits in subset})}$;

means for ~~providing~~ outputting the sum as a first multiple bit value ~~of a second signal~~; and

means for receiving a second plurality of bits from the ~~first~~ signal and converting to a second multiple bit value ~~of the second signal~~ using the steps described above until all bits in the ~~first~~ signal have been converted, wherein each plurality of bits has the same number of bits and each subset of bits in the plurality of bits has the same number of bits.

23. (Previously Presented) An apparatus for conversion of a direct stream digital signal to a pulse code modulated signal, comprising:

a first-in-first-out (FIFO) buffer that contains said direct stream digital signal;

a table coupled to the FIFO buffer, wherein a plurality of look-ups are performed in the table based upon subsets of bits of said direct stream digital signal to create a sum; and

an accumulator coupled to the table, the accumulator creating said pulse code modulated signal based upon said sum.

24. (Cancelled)

25. (Currently Amended) A method for conversion of signals, comprising:

building a look-up table, said table containing a plurality of partial sums, ~~The method of claim 24,~~ wherein building the look-up table comprises:

allocating a two dimensional array containing a plurality of elements, wherein said two dimensional array has a first dimension and a second dimension;

computing for each element of the first dimension in the array a partial sum for each bit pattern over a sequence of bit patterns from 00...000bin to $(2^{(\text{number of bits in a word})}-1)$bin;

storing the partial sum for each bit pattern over ~~the~~ a sequence of bit patterns in the corresponding element of the second dimension;

receiving a first signal;

performing a plurality of look-ups in the table with words from the first signal to determine partial sums;

adding the partial sums to create a total sum; and

outputting the total sum as a multiple bit value.

26. (Previously Presented) The method of claim 25, wherein the size of the first dimension in the two dimensional array is equal to the number of words in the first signal, the size of the second dimension equal to $2^{(\text{number of bits in a word})}$.

27. (Previously Presented) The method of claim 25, wherein each element of the first dimension in the array has a plurality of coefficients, each of said coefficients corresponding to a bit position in the bit pattern.

28. (Previously Presented) The method of claim 27, wherein computing the partial sum for each bit pattern comprises:

determining the value of the bit in the i^{th} position of the bit pattern;

adding the coefficient corresponding to the i^{th} position of the bit pattern to the partial sum if the value of the bit is one;

subtracting the coefficient corresponding to the i^{th} position of the bit pattern from the partial sum if the value of the bit is zero; and

generating the partial sum for the bit pattern after adding or subtracting the coefficients corresponding to each bit in the bit pattern.

29. (Currently Amended) The method of claim 25, wherein the partial sum for each bit pattern is stored in the element of the second dimension corresponding to ~~the~~ a value of the bit pattern.

30. (Previously Presented) A method of converting a direct stream digital signal into a pulse code modulated signal, comprising:

receiving said direct stream digital signal;

performing a plurality of look-ups in a table based upon subsets of bits of said direct stream digital signal to create a sum; and

creating said pulse code modulated signal based upon said sum.

31. (Previously Presented) The method of claim 30, wherein each of the subsets of bits is the same number of bits.

32. (Currently Amended) The method of claim 31, wherein the table is a two dimensional array containing a plurality of elements, the size of the first dimension equal a number of bits in the direct stream digital signal divided by ~~the~~ a number of bits in the subset of bits, the size of the second dimension equal to $2^{(\text{number of bits in subset})}$.